

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Hiroyuki Nakajima	Examiner:	Unassigned
Serial No:	Unassigned	Art Unit:	Unassigned
Filed:	Herewith	Docket:	17472
For:	PROCESSOR, SYSTEM LSI CIRCUIT, METHOD OF DESIGNING SAME, AND RECORDING MEDIUM HAVING SAID METHOD RECORDED THEREON	Dated:	February 24, 2004

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450
Attn: Mail Stop New Applications

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. Japanese Patent Kokai Publication No. JP-A-8-106383, dated April 23, 1996; and
2. Japanese Patent Kokai Publication No. JP-P2002-328804A, dated November 15, 2002.

CERTIFICATE OF MAILING BY EXPRESS MAIL

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I hereby certify that this correspondence is being deposited with the United States Postal Service Express Mail Post Office to Addressee service under 37 C.F.R. §1.10 on the date indicated above and is addressed to the Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: February 24, 2004



Paul J. Esatto, Jr.

Applicant is submitting copies of the above-cited references. The relevance of the above-identified references has been described in the specification.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,



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